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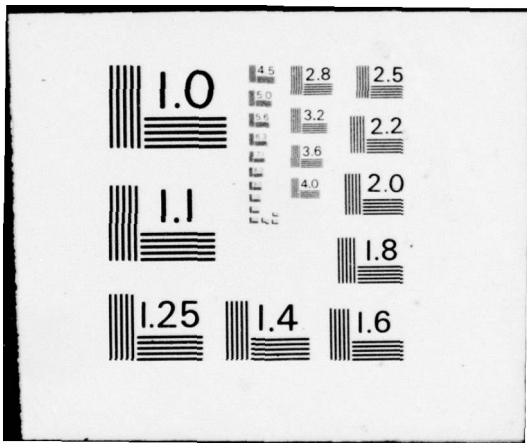
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DEVELOPMENT, FABRICATION AND SERVICE OF INSTRUMENTS FOR USE IN ELECTRICAL STRUCTURES AND RELATED SPACE FLIGHT MEASUREMENTS

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Scientific Report No. 1

28 May 1976

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The goals established at the onset of this program were fourfold: (1) design and fabricate, (a) a spherical electron sensor, (b) a planar ion sensor, (2) design and fabricate a low voltage power converter, (3) design and develop a nine (9) bit successive approximation ADC, (4) design and build suitable test equipment for thorough testing of the SS/IE plasma electronics.

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SUMMARY

The goals established at the onset of this program were fourfold: (1) design and fabricate, (a) a spherical electron sensor, (b) a planar ion sensor, (2) design and fabricate a low voltage power converter, (3) design and develop a nine (9) bit successive approximation ADC, (4) design and build suitable test equipment for thorough testing of the SS/IE plasma electronics.

The most noteworthy achievements concern the variety of assembly techniques tried and subsequently rejected in the early phase of the planar and spherical sensor development. This phase pointed out that the simpler a technique is, the more reliable and easier it is.

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LIST OF FIGURES

1.0 Analog to Digital Converters and Multiplexing Logic

The Analog to Digital Converter (ADC) and multiplexing logic is comprised of four sections, (1) input/output logic buffers, (2) formatting logic, (3) ADC subsection logic, (4) serialization logic.

1.1 The Input/Output Logic

These buffers consist of a quad LM 139 voltage comparator integrated circuit, shown in Figure I, section 1.1. The functions of these broad threshold circuits is to allow for a large excursion on the interface signals with no apparent degradation in system performance.

1.2 Formatting Logic

The formatting logic, Figure II, section 1.2, is that part of the design which accepts the 10KHz from the interface buffer circuit, and subsequently counts this signal down to produce a 20Hz squarewave.

The countdown logic C1, C2, C3, and C5 is divide by ten, five ten, and three circuits, the output of this chain is the 20Hz squarewave which multiplexes the three analog inputs into the ADC. The multiplexer circuit (M1) is a four channel CMOS analog switch which has a R_{on} of less than ten ohms thus affording minimum attenuation loss on the sensor input lines.

1.2.1 ADC Control

The ADC Control contains the logic required to turn the analog processor and oscillator on and off, synchronous with the input multiplexers.

1.3 ADC Subsystem Logic

The ADC subsystem logic, Figure II, section 1.3, is the central portion of the data processor. Its function is to input the analog signals from the sensor multiplexer (M1) and translate this voltage into an equivalent nine (9) bit binary number.

This process commences when the ADC Control (Section 1.2.1) issues a signal to the one (1) MHz oscillator and the sequencer to "START". This start signal enables the oscillator, and resets the sequencer to its zero state which in turn initializes the ADC register. The sequencer is

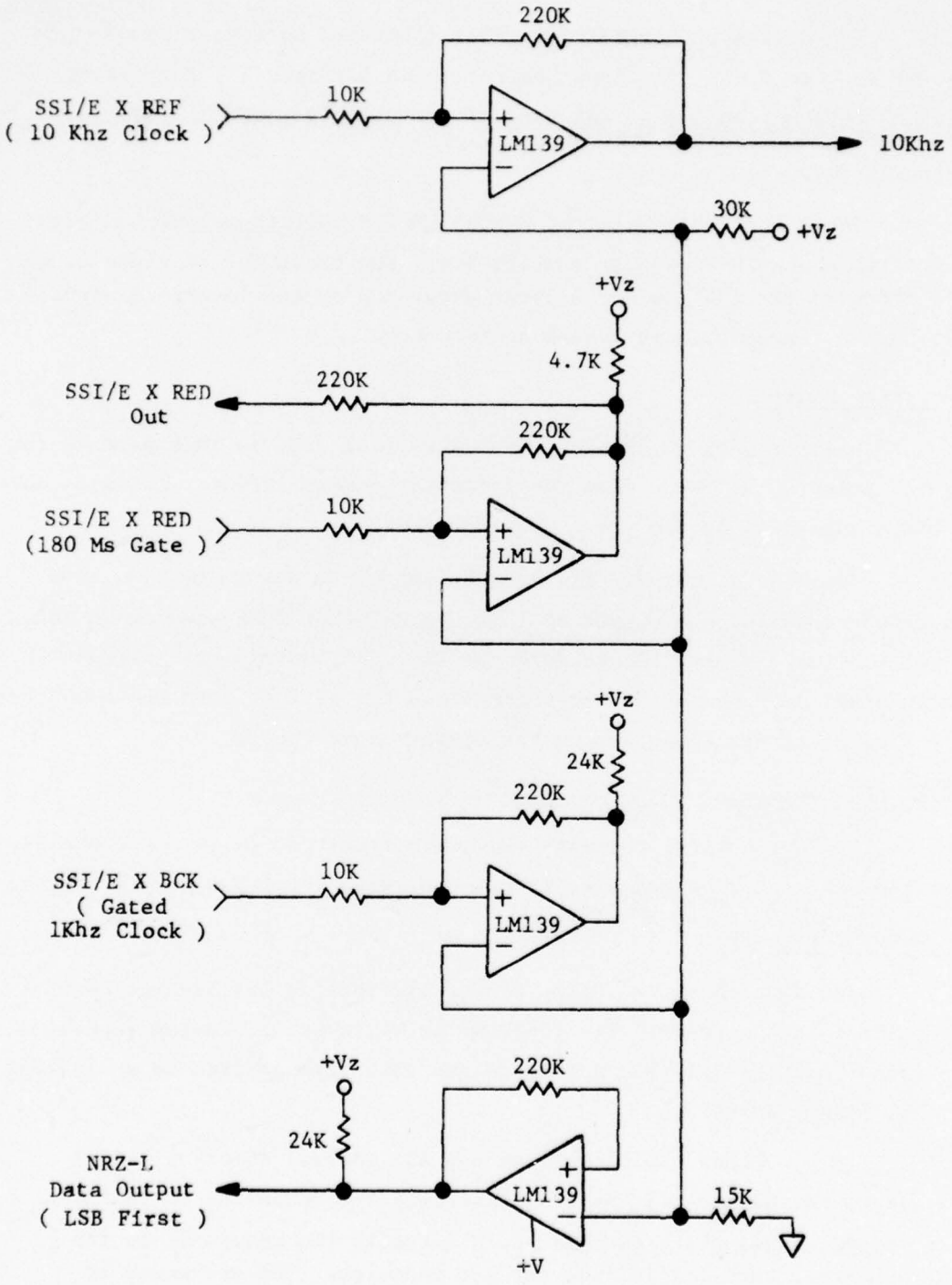


Figure I Interface Buffers

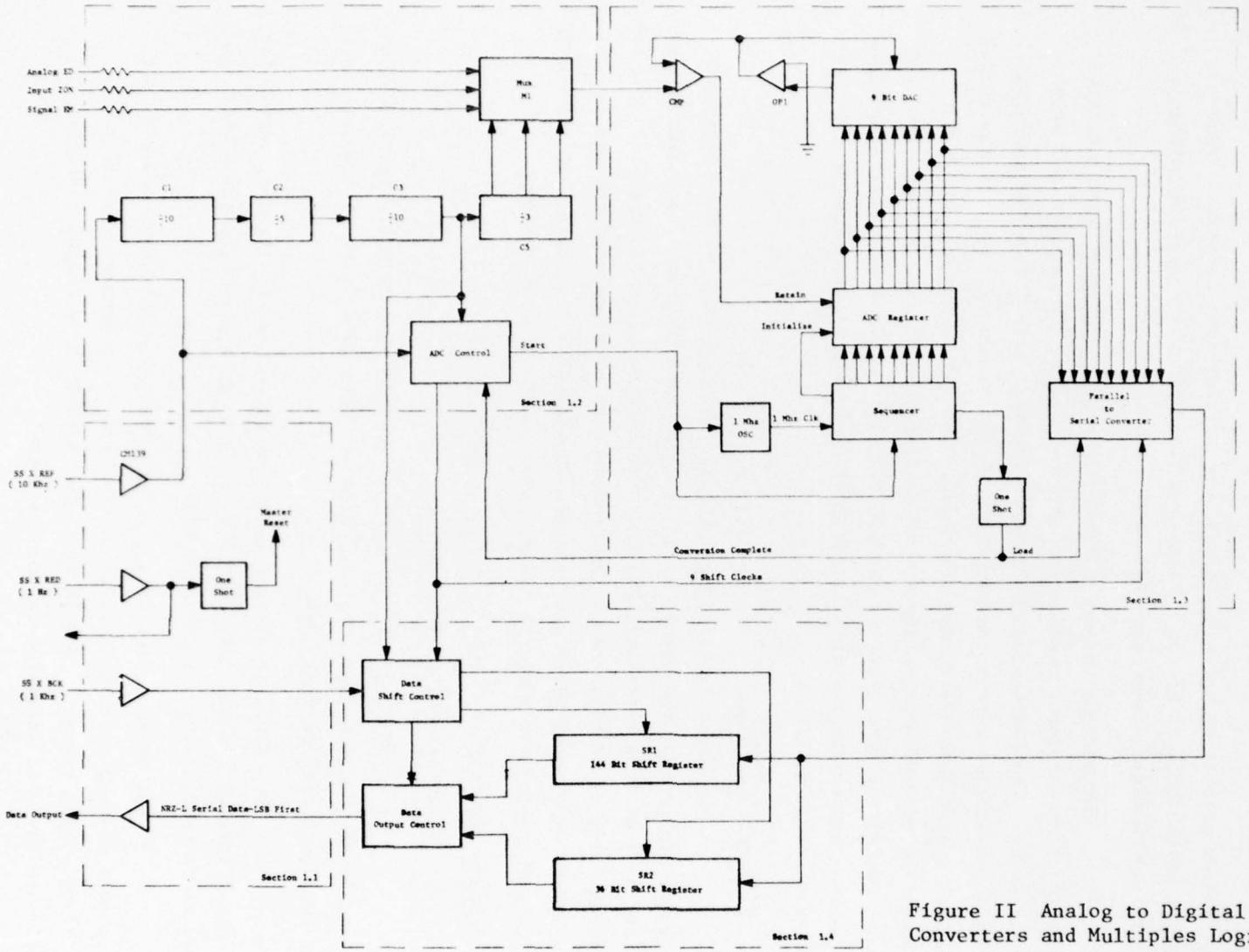


Figure II Analog to Digital Converters and Multiples Logic

comprised of a chain of three (3) decode counters/divider circuits. These circuits switch on (one bit at a time) a series of current sources inside the Digital to Analog Converter (9Bit DAC).

The current output of the 9 bit DAC is converted into a voltage proportional to the input current and compared against the multiplexed sensor input voltage. The Comparator (CMP) makes the decision between the magnitude of the input voltage versus the magnitude of the Op Amp voltage - if the sensor input is greater than the Op Amp OPI input, that bit of the ADC register causing this to happen is retained - if the converse of that is true, this bit is removed and the next lower weight bit is tried. This process continues until the maximum conversion accuracy is obtained, which is a conversion to the nearest ten (10) millivolts.

1.4 Serialization Logic

The serialization logic, Figure II, Section 1.4, has a dualfold function. (1) Accept the twenty words of data which have been digitized by the ADC and shifted into registors, SR1 and SR2. SR1 is a 144 bit register, the other register, Sr2, is 36 bits long. (2) Provide a holding register for the 180 bits of data and under control of the data output control logic shift this information to the PCM encoder for ultimate transmission to the ground stations.

1.5 Plasma Electronics Ground Support Equipment (GSE)

1.5.1 Signal Simulator Electronics

The functions of the signal simulator electronics, Figure III, is to provide an identical spacecraft interface. This capability will insure an easy experiment integration phase.

The simulator section generates three digital signals, namely ten kilohertz reference clock (SS x REF), a one kilohertz bit clock (SS x BCK), and a one hertz readout gate clock (SS x RED).

The source clock is a 1.28 MHz Vectron oscillator, whose output is counted down by circuits C1, C2, C3, C4, and C5 to generate the aforementioned timing signals. The three timing signals have output circuits which simulate that generated by the spacecraft.

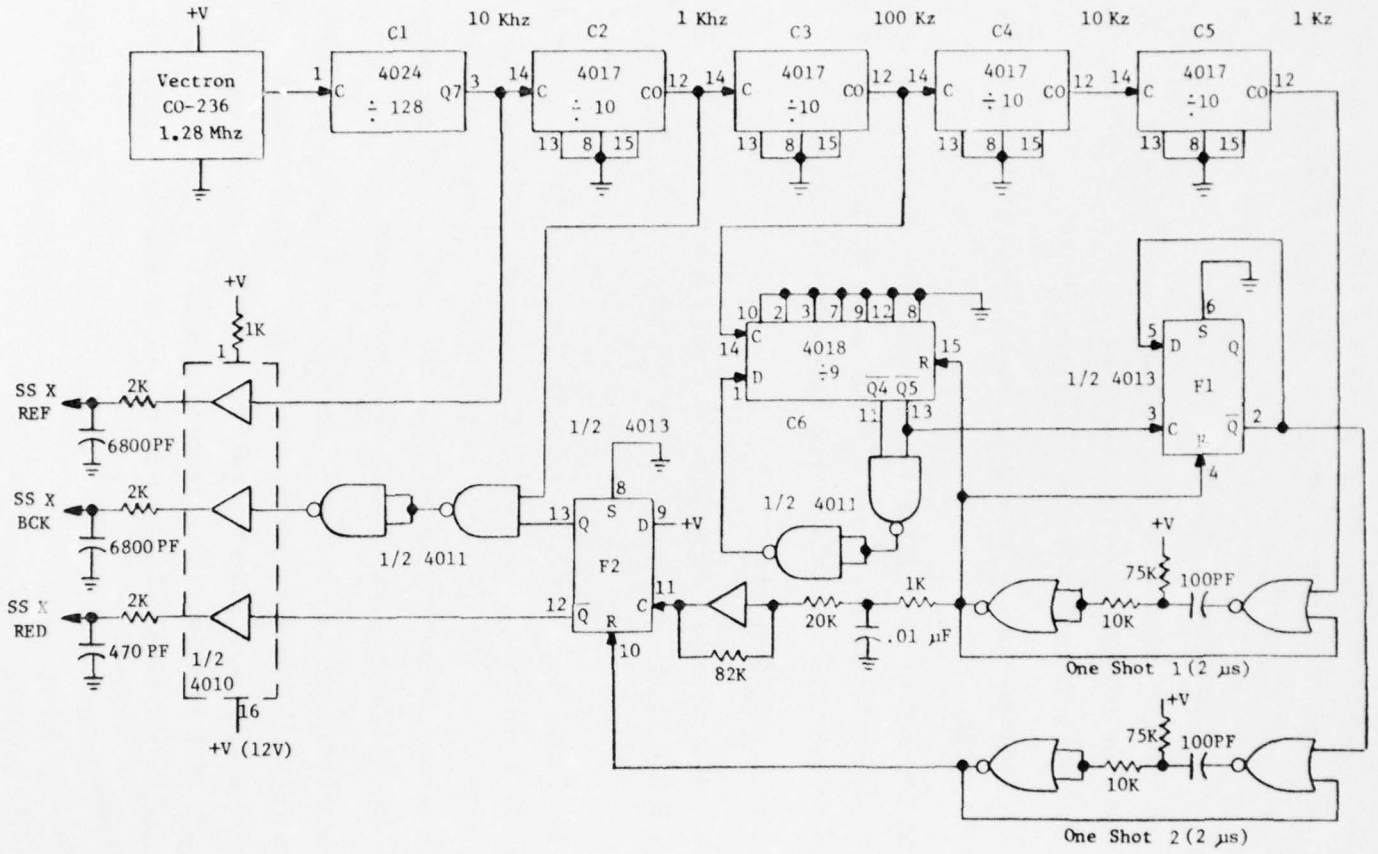


Figure III Signal Simulator

1.5.2 Display Electronics

The display section, Figure IV, of the GSE may be treated in three sections: (1) Input Data Shift Registers, (2) Data Selectors, and (3) Display Sections.

1.5.2.1 Input Data Shift Register

The 180 bit input data shift register is analogous to the serialization logic (Section 1.4) in that this chain of logic provides temporary storage of all the data the ADC processor supplies to it.

The register is 180 bits long and the data in it is shifted under control of the SS x BCK.

At the end of this gated clock train, the positive going edge of the readout gate inhibits any further data from being shifted into the holding register and transfers this new data to the data selector logic.

1.5.2.2 Data Selectors

The data selector logic and the word selector switches together determine which 9 bit block of data is to be displayed on the three digit output display.

The function of the word selector switch is to provide a three bit code to the data selector logic; with this code the data selector logic can determine which input of eight sources is to be displayed. The word selector switch is set up in such a fashion that the selection of the word "zero" displays zeros on the LED readouts (Light Emitting Diode).

Selections of the words one through seven routes the corresponding scientific data from the input data register to the readout display. The remaining positions of the word selector switch, positions eight and nine, are used for the lamp test feature. This feature automatically selects the number "eight" which checks all seven elements of the seven segment display in the readout mechanisms.

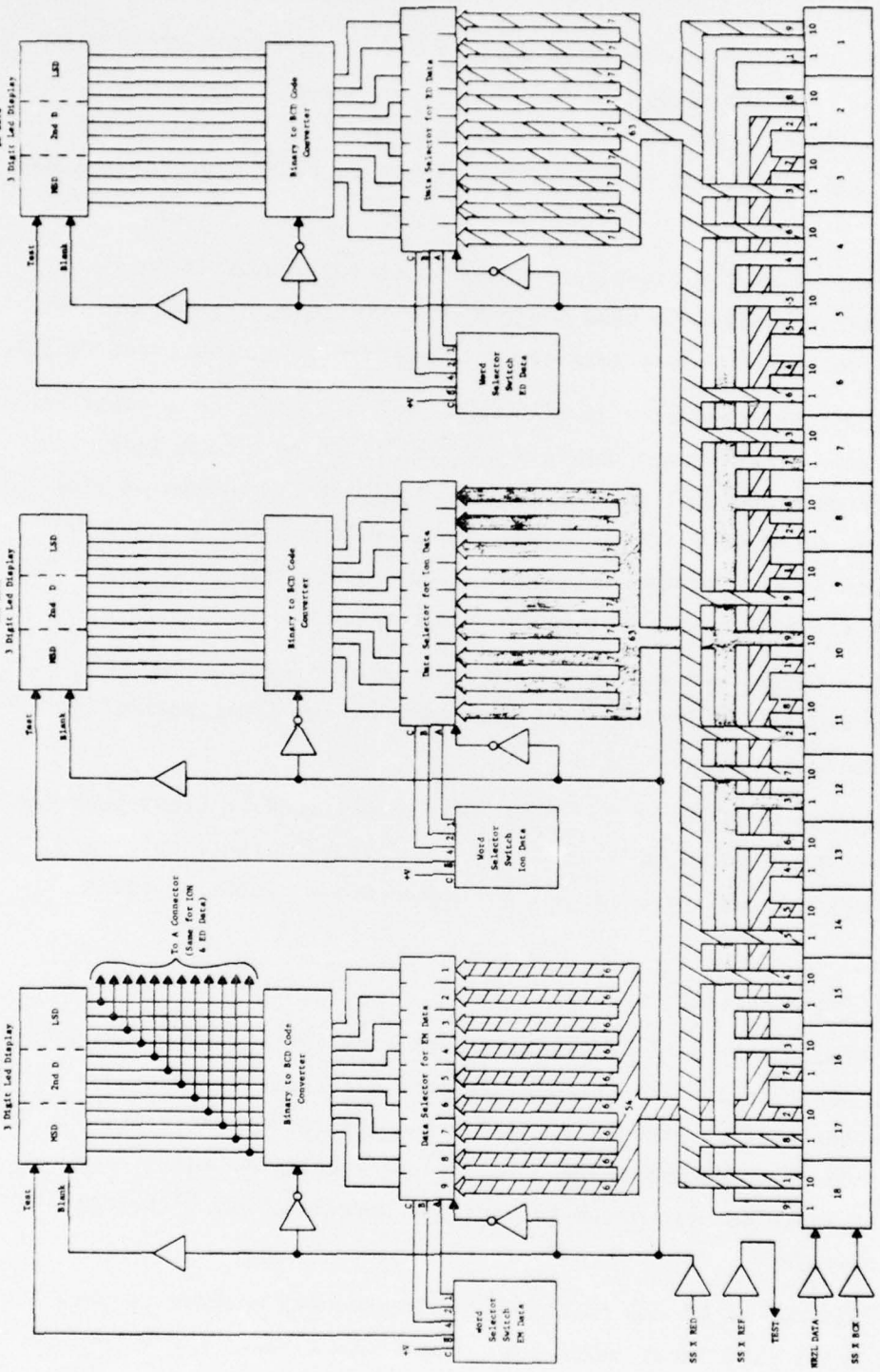


Figure IV Display Section

1.6 Introduction

The low voltage converter used to power the PLASMA EXPERIMENT has been designed with circuitry and components used in many successfull space flight converters. The design is based on providing the best reliability, weight, and efficiency while meeting all of the specified performance requirements.

Because of the relatively small input voltage variations, a dissipative linear regualtor is used instead of a switching regulator. This results in less reflected noise, less complicated circuitry, and lower weight.

The power converter is commanded "on" and "off" by a power enable signal. The status of the power converter is indicated by a high (+5V) for an off condition or a low (0V) for an on condition. The converter is protected against overloads or short circuits across the outputs as well as internal circuitry. There is also protection against the application of reversed voltage or high voltage transients at the input to the converter.

The weight and size of the system is kept low through the use of the Spacetac modular approach. This technique allows dense packaging without impairing maintainability.

Specific attention has been paid to eliminating noise problems which constantly arise in DC to DC converters. Circuit layout, shielding, and filters have been designed to attenuate reflected noise, radiated noise, and ground noise.

1.6.1 Circuit Description

Figure V is a block diagram of the Low Voltage Power Converter. The +28V input power is applied through the enable circuit to the input filter. This filter is designed to prevent bus noise and ripple from entering the converter and minimizes conducted noise being fed back onto the bus. Radiated noise from the supply is attenuated by adequate shielding and high frequency bypassing to chassis.

The output of the filter is simultaneously applied to both the start circuit and to the input regulator. The start circuit feeds the reference diode which causes the output of the amplifier to go positive, thereby

causing the series pass element to turn on. The start circuit output is also applied to the saturating magnetic oscillator which provides a squarewave output.

The transistor bridge chopper receives its drive from the oscillator and starts chopping the output of the series pass transistor and applying this AC voltage to the primaries of output transformers T1 and T2. Transformer T1 provides the higher power output voltages as well as the bias and feedback voltages required by the primary circuitry. T2 provides the balance of output voltages. Once the feedback voltage of T1 has reached a preset level, the regulator will hold the voltage across this winding constant, thus providing the desired primary regulation. Once the voltage on the transformer is high enough, rectified bias windings provide a more efficient means of supplying internal voltages and bias the start circuit off.

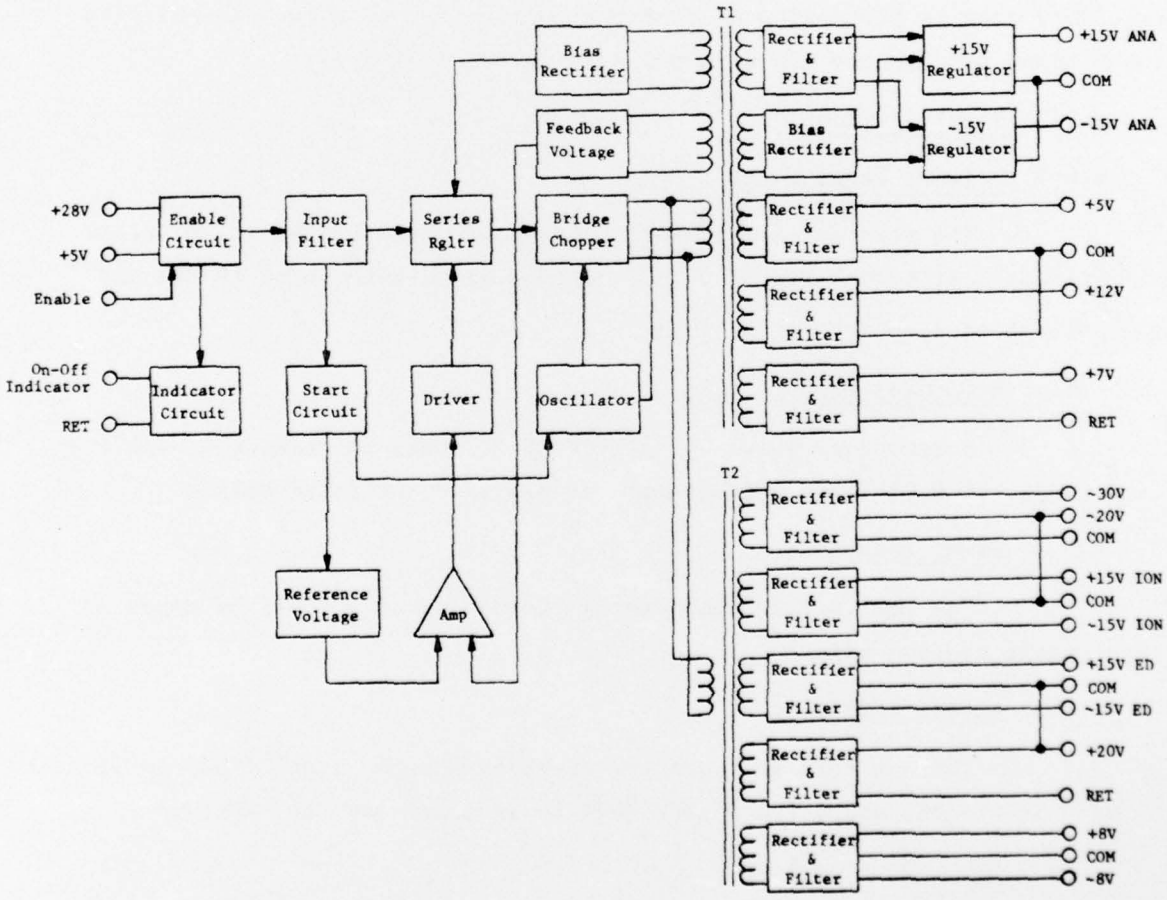


Figure V Low Voltage Power Converter

The secondary windings of the power transformers are rectified and filtered to provide the required output voltages. The ±15V analog outputs are applied to post regulators prior to being brought out. The operation of these output regulators is the same as the primary regulator.

All outputs which do not require post regulation utilize C-L-C output filters with additional ceramic capacitors located at the output terminals for high frequency bypassing. The power transformers also contain shields which enclose primaries and secondaries in order to minimize noise coupling.

The regulators contain protection against overload and short circuit. The primary regulator limits the current which can be drawn from the input bus due to internal shorts or short circuits across unregualted outputs. Each of the post regulators will limit the current which can be drawn due to a short circuit or overload at their respective outputs. In addition, the power converter is protection against the application of a reverse polarity at the input through the use of a polarity reversal diode.

1.6.2 Specifications

1.6.3 Primary Input Power

The primary input power to the converter is +28V ±0.56 Volts. In addition, a sine wave ripple of 0.1 volts peak-to-peak up to 19 MHz may be superimposed upon the primary unit.

1.6.4 Secondary Power

A secondary power bus of +5V ±0.25 volts containing a superimposed ripple of 0.05 Volts peak-to-peak is provided for power enable.

1.6.5 Power Enable

The low voltage converter is commanded on and off by means of a power enable control signal.

1.6.6 On-Off Indicator

The low voltage converter provides a high signal (+5V) to indicate an "off" condition, and a low output (0V) to indicate and "on" state.

1.6.7 Output Power

Output Voltage (V)	Function	Current (mA)	Regulation %	Ripple (mV)	Spike (mV)
+15	Analog	15	±0.5	1	10
-15	Analog	30	±0.5	1	10
Common'					
+5	Digital	7.5	±5.0	1	10
+12	Digital	2	±5.0	50	100
Common'					
+7	Relays	23	±5.0	10	--
Common'					
+15	ED	3.5	+1.0	1	10
-15	ED	5.5	±1.0	1	10
Floating					
+15	Ion	4.2	±1.0	1	10
-15	Ion	4	±1.0	1	10
Floating					
-20	Ion	0.2	±5.0	5	10
-30	Ion	0.01	±5.0	5	10
Floating					
+20	ED	0.2	±5.0	5	10
Floating					
+8	Digital	20	±5.0	10	50
-8	Digital	20	±5.0	10	50
Common					

Notes: 1. The separate analog and digital commons are tied together at the experiment.

1.7 Spherical Electron Sensor Task

The design and fabrication of a Spherical Electron Sensor with a globe shaped collector mounted within, completely insulated from a spherically shaped outer grid, was the goal. These globes are fastened to a shaft which contain conductor leads soldered to an interface connector and mounted on the spacecraft boom.

1.7.1 Physical Requirements

1.7.1.1 Dimensions

1. Outer grid 2.250 dia.
2. Collector 1.750 dia.
3. Shaft .500 dia. x 1.500 long. (between boom mount and grid), which is divided into 3 parts: insulator, guard ring, and insulator (.500 long each).

1.7.1.2 General Requirements

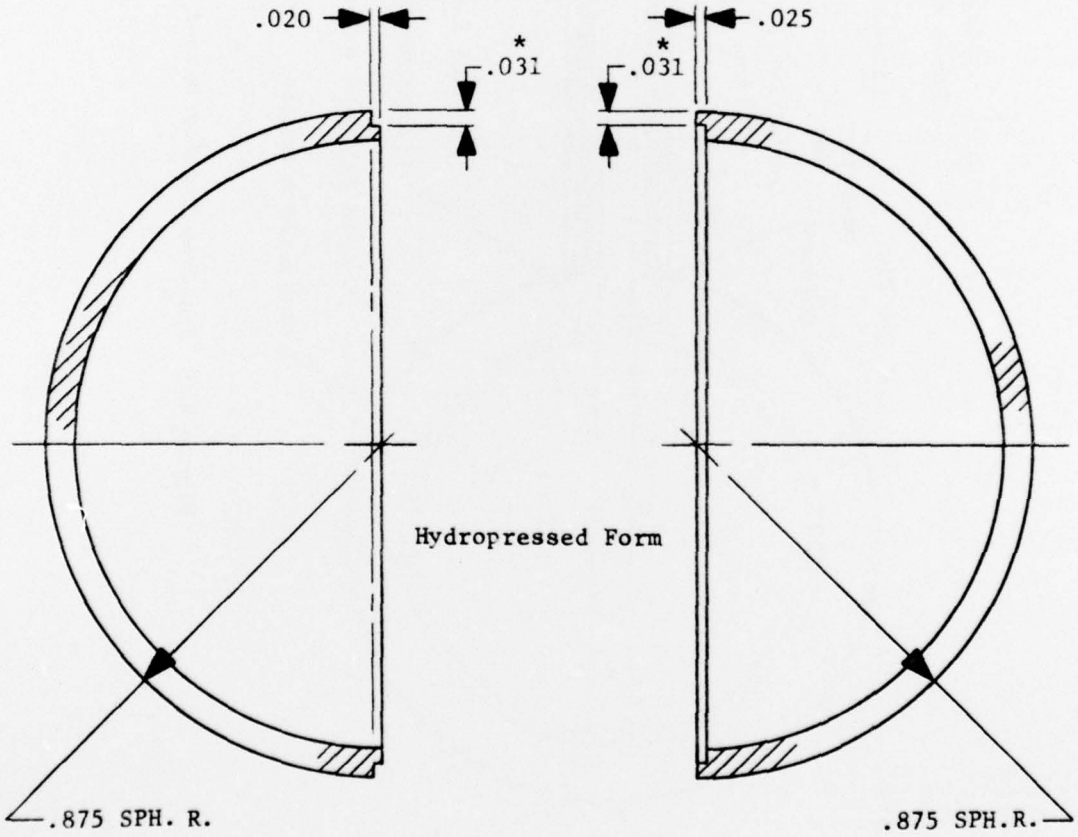
1. The unit will weigh a max. of 75 grams.
2. The spheres will be concentric within $\pm$10% of each other.
3. Where required, insulators used must have at least 10^{12} ohms of resistance.
4. The grid will be made from a material which is a minimum of 70% open face and be a good conductor.
5. The collector will be made from a material which is a good conductor.
6. Devise a way of fastening the sensor to the spacecraft boom.
7. Design a quick disconnect interface connector.
8. A guard ring will be provided on the shaft and be connected electrically to the grid.
9. The guard ring material will be made from a good conductive material.
10. All mating metalic parts must be of the same material or plated with the same finish, preferably gold.

1.7.2 Problem Areas

The most problematic area associated with the Spherical Electron Sensor was the design of a grid which would meet the requirements of Section 1.7.1.2 Grid Halves A & B and collector assembly.

The first task was to find a material for the grid. With advice from an agency specialized in metal forming, we selected half hard brass and had perforations etched on .006 thick sheets. After several attempts to form the hemispheres, with little success due to material fractures, this approach was abandoned.

We ultimately found that hydroforming was the most successful method (See Fig. VI).



*Both Halves to Fit Together

Figure VI Collector Halves Electron Density Sensor Phase 2

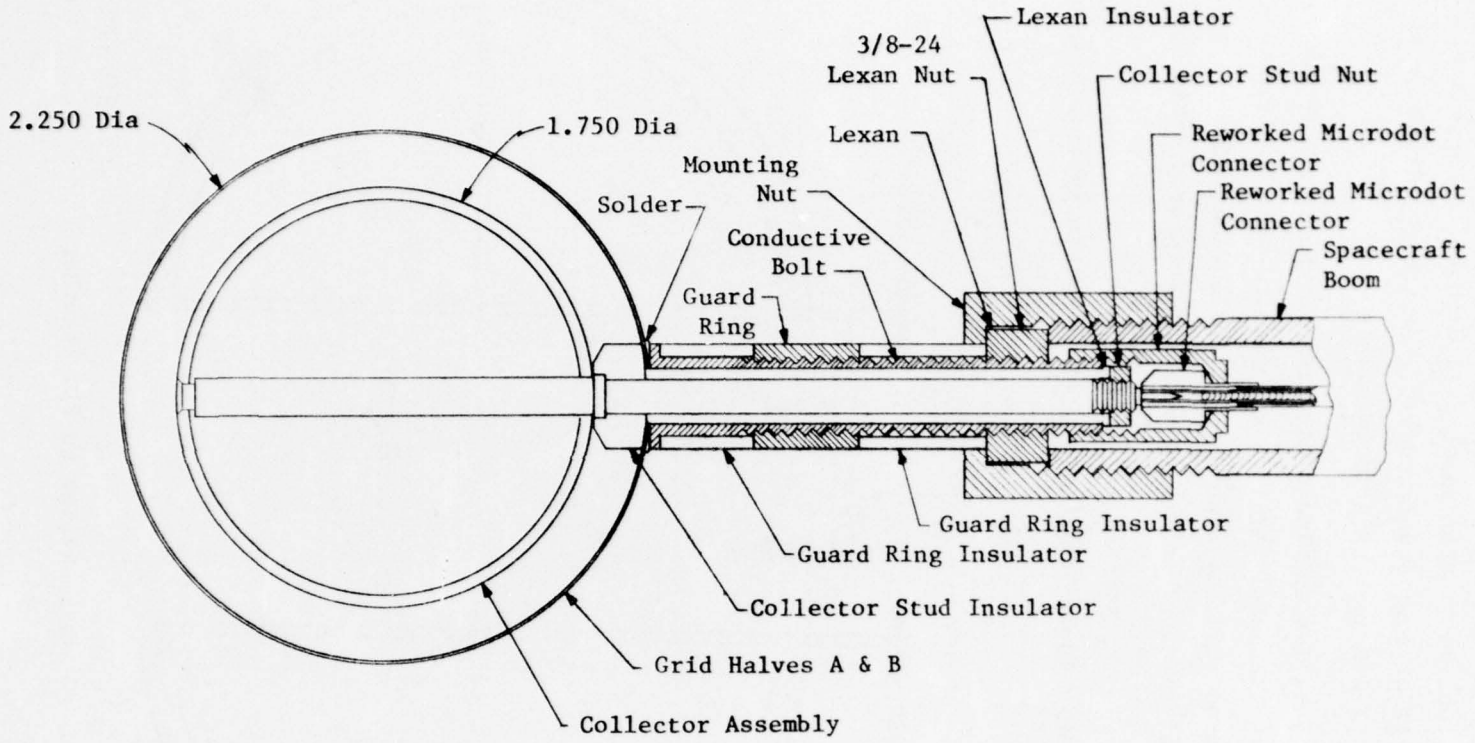


Figure VII Electron Density Sensor Assembly

Lexan proved to be a good insulator and the decision to use it for all insulation problems seemed troublefree.

The use of machined metal pieces between the spheres and connector negated the need of wire.

A Microdot connector was reworked to meet our servicing needs, See Figure VII.

The boom mount and boom's end design was defined and easily configured. (See Fig. VIII & IX).

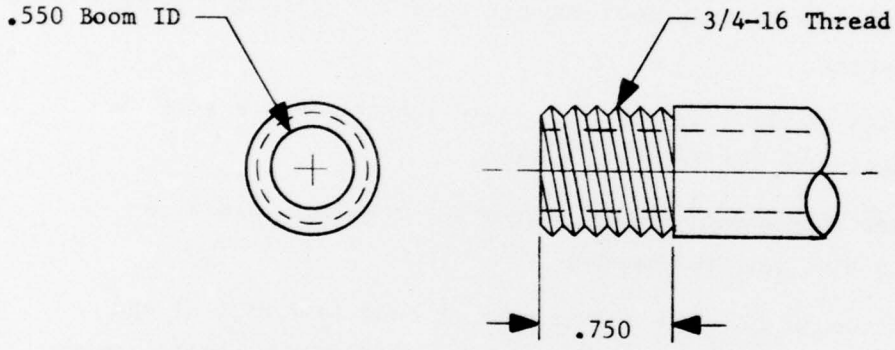
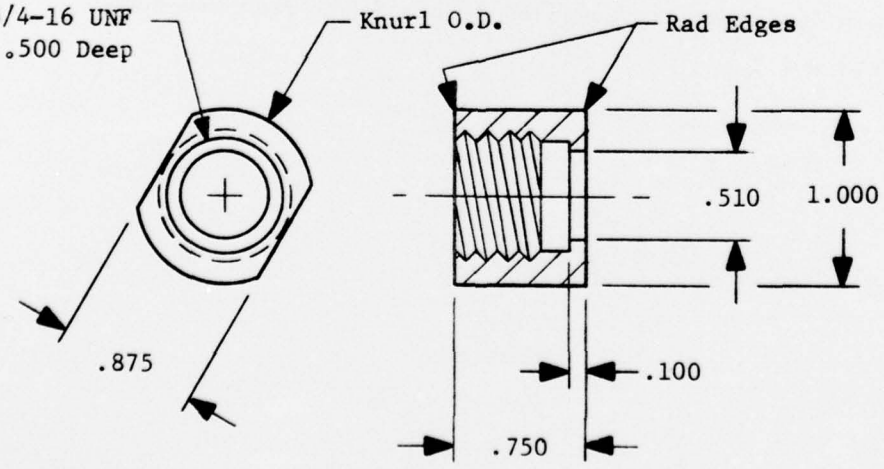


Figure VIII Spacecraft Boon Electron Density Sensor



NOTES

1. Gold Plate (Including Thread) .00005 THK.

Figure IX Mounting Nut Electron Density Sensor

A continuing search for a grid material yielded a #18 stainless steel mesh with .006 wire easily formed into hemispheres that could be deformed and easily returned to proper shape.

The design of a grid using the stainless steel mesh with a support system of three circular bands to form a sphere.

The use of all stainless steel pieces minimized any dissimiliar metal problems.

The design was now ready for a prototype evaluation model for customer approval.

The customer (AFGL) rejected the grid design. They suggested we redesign the grid using only 360° support band, to increase the percentage of open area.

A redesign of the grid using a single support band was fabricated and sent again for customer evaluation.

A further increase of the open area was required, hence, a reduction in band size was implemented.

A reduction in the size of the support band (See Fig. X) and a change in most of the metal pieces to aluminum afforded a weight saving of approximately 80 grams. A Gold plate finish on all metal parts allowed submittal of our completed redesign to the customer (See Fig. VII).

This design was approved by AFGL and all required sensor housings were built.

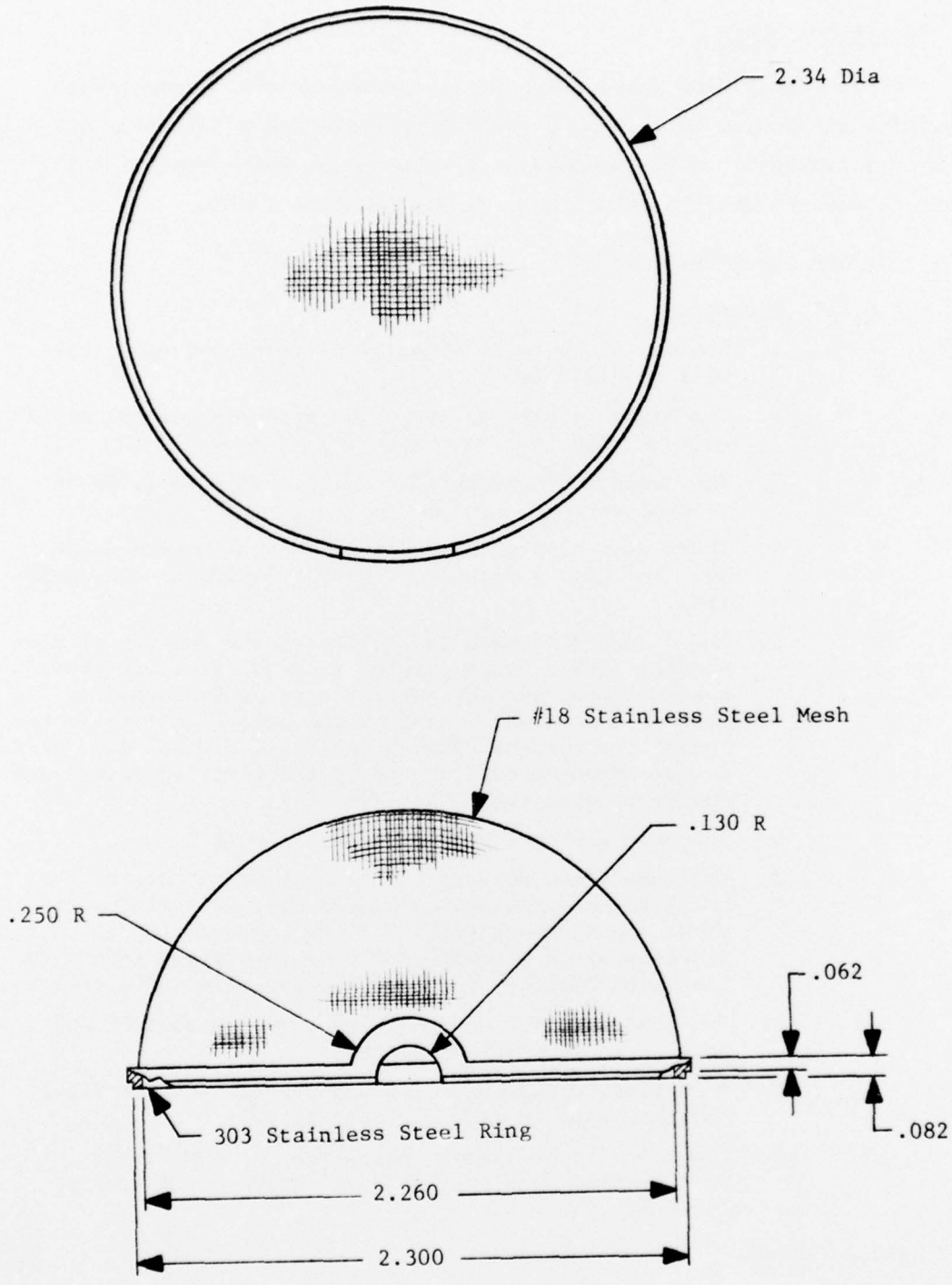


Figure X Grid Assembly Half

1.8 Ion Sensor Scope

The design and fabrication of Ion Sensor (Planar Sensor) with a cylindrical housing containing 3 round flat grids and a collector all wired to a cannon connector mounted at the bottom of the cylinder on the interface surface was the second requirement for sensor work.

1.8.1 Physical Dimensions

1.8.1.1 Dimensions

1. The maximum outside diameter of grids and collector will be 3.000 in.
2. The distance between the grid, and grid and collector will be .250 in.
3. The collector's conductive surface will be 2.500 in. in diameter.
4. There will be 3 grids, 2 of which will have a 2.500 in. dia. grid area and one with a 2.000 in. dia. grid area.
5. The distance between the collector and the top of the housing should be no greater than the distance between the collector and the intersecting angle formed by drawing a straight line from the edge of the collector's conductive surface through the two 2.500 in. dia. grids to the opposite edge of the aperature's (uppermost and smallest) grid area. (See Fig. XI).
6. The unit must weigh less than 300 grams.
7. The insulation between the conductive surface of the collector and the mating pieces must be a minimum of 10^{12} ohms. Epoxy board (G10) will be approved for all other insulators. A minimum amount of insulation should be lining the inside of the sensor for scientific reasons.
8. The grid material used must be a good conductor and have at least a 90% open area.
9. The grids (when mounted in the sensor) must be tight and flat without tears or separations.
10. The 2.500 inch diameter grids must be completely insulated from each other and all other components of the unit.

1.8.2 Problem Areas

The only problem area encountered was that of proper insulation between the collector and grid structure.

1.8.3 Design Efforts

1. The first effort was to improve on the collector design (earlier designs were hand made and difficult to assemble). A design using a gold plated copper, kapton, and G10 laminate for the collector portion was implemented. The copper was etched to form the collector and insulated from the unit by a layer of kapton backed by G10. All the collector pieces were fabricated using standard printed circuit techniques thus simplifying the assembly.

2. Grids were assembled using different meshes stretched over and epoxied to etched nickel rings. To insulate the 2.500 in. dia. grids, the enclosed erea was encapsulated with kapton. The grid material previously used proved to be the best and was called for in the design.

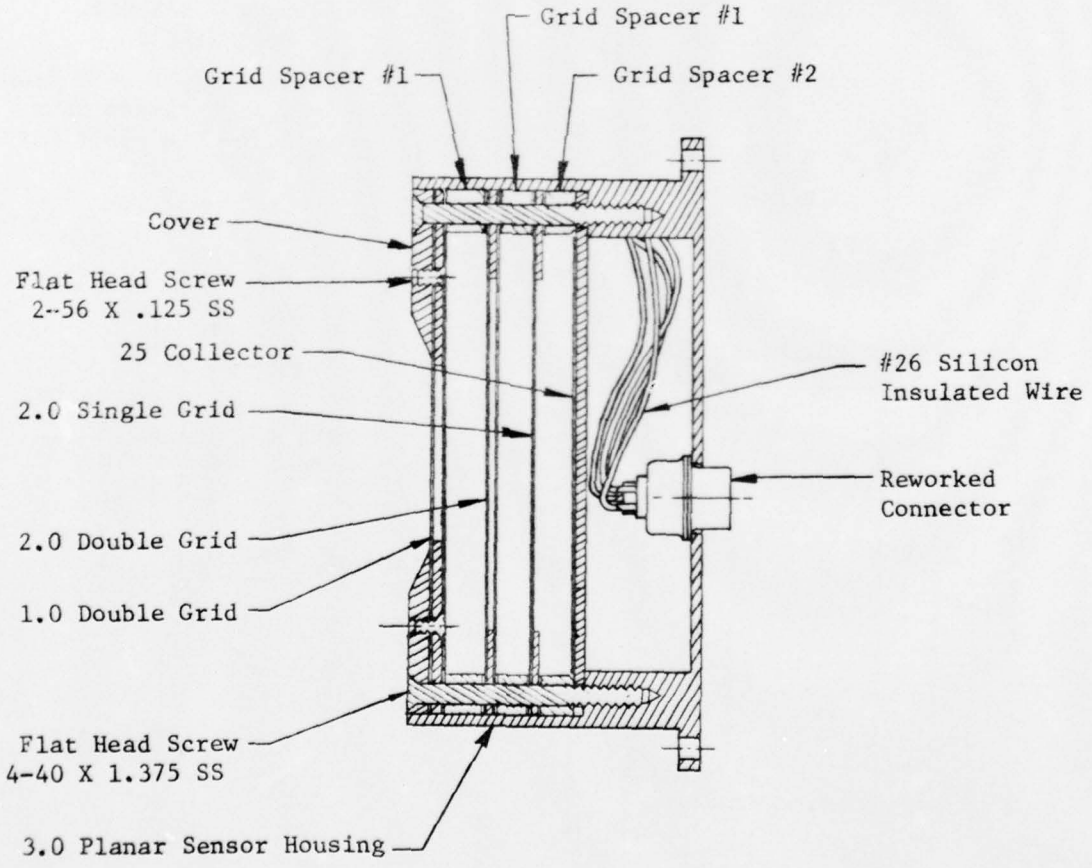


Figure XI 3.0 Planar Sensor Assembly Phase 2

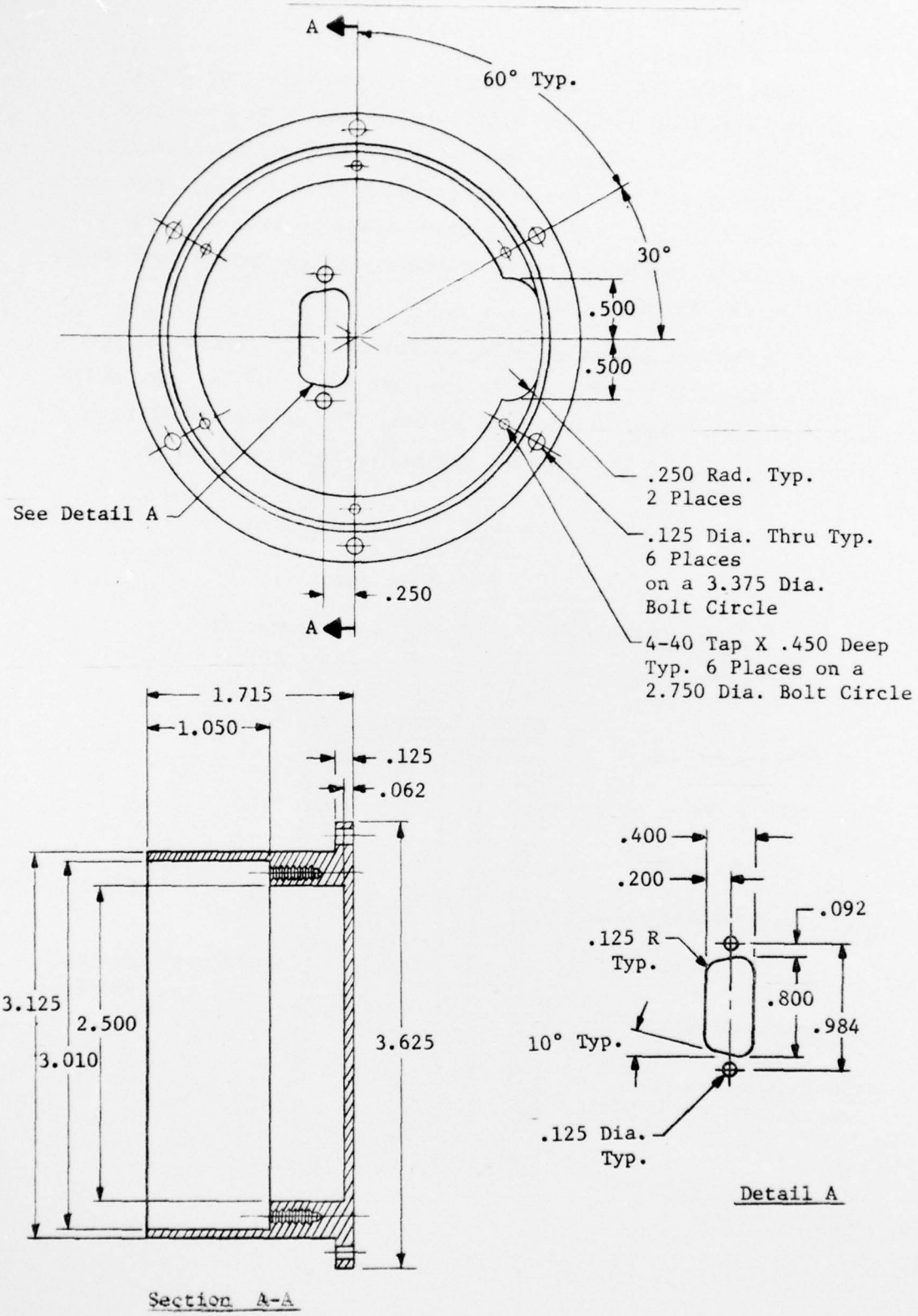


Figure XII Housing 3.0 Planar Sensor Phase 2

3. The housing design was a simple can shape closed on one end, with boom interface mounting flange at the bottom encircling the outside diameter of the cylinder providing a means of fastening the assembly to the spacecraft. A grid/collector mounting shelf was located on the inside diameter and a connector mount at the bottom. (See Fig. XII).

4. Metal rings were designed as spaces to separate and locate the grids and the collector. (See Fig. XI).

5. The initial design was completed and sent to AFGL for review. This design proved adequate and a prototype was made.

6. The following changes resulted from prototype evaluation:

   a) The grid open area was changed from 2.000 dia. to 1.000 dia. on the aperature grid and from 2.500 dia. to 2.000 dia. on the others.

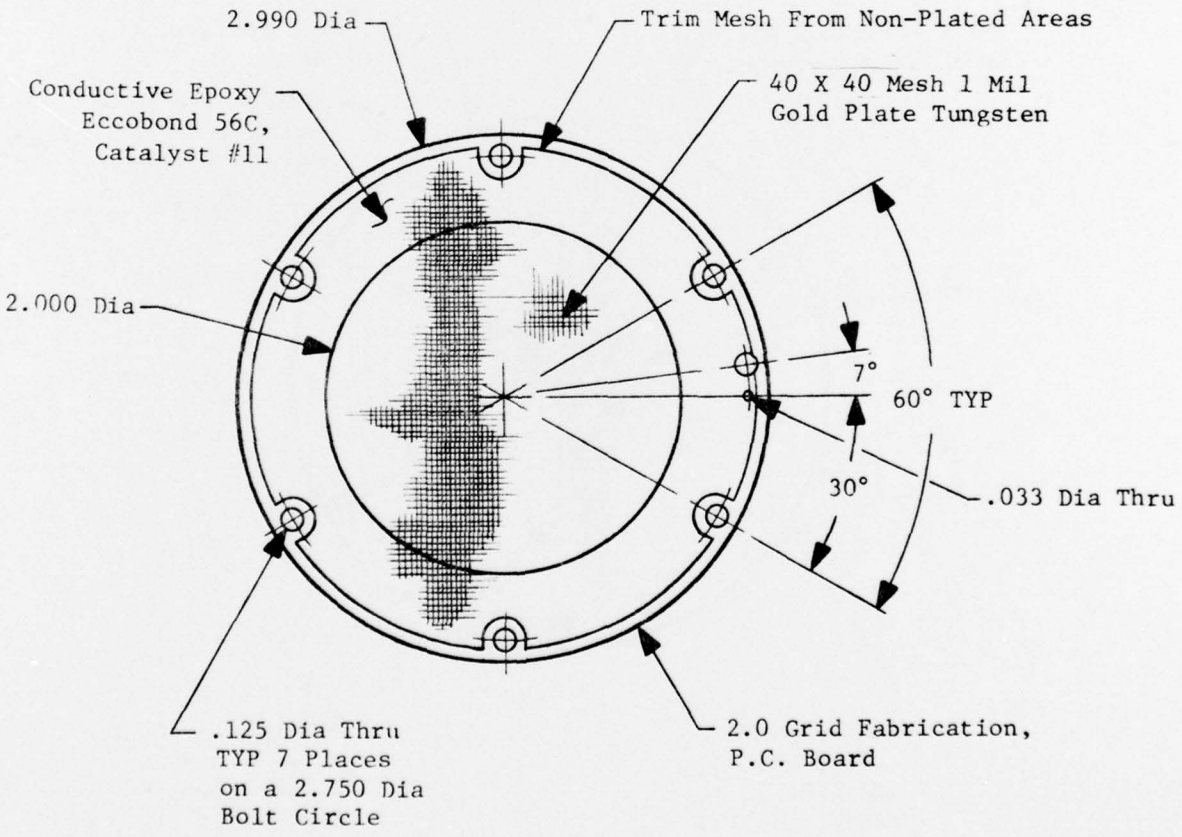


Figure XIII 2.0 Grid Assembly 3.0 Planar Sensor Phase 2

b) The aperature grid and one of the 2.000 dia. grids were changed from grids with mesh on one side to grids with mesh on both sides. The two meshes had to be separated by about 1/32".

c) A cover was required.

7. The grids were redesigned using 2 sided copper clad G10 (etched as shown in Fig. XIII and XIV), with the meshes mounted as they were when we used nickel rings. Successful fabrication of the first grids was achieved but an attempt to repeat the process failed to happen, for unsatisfying reasons.

8. Experiments were conducted in applying mesh using epoxies and was found to be very difficult, but had eventual success using solder to affix the grid material allowed completion of this task.

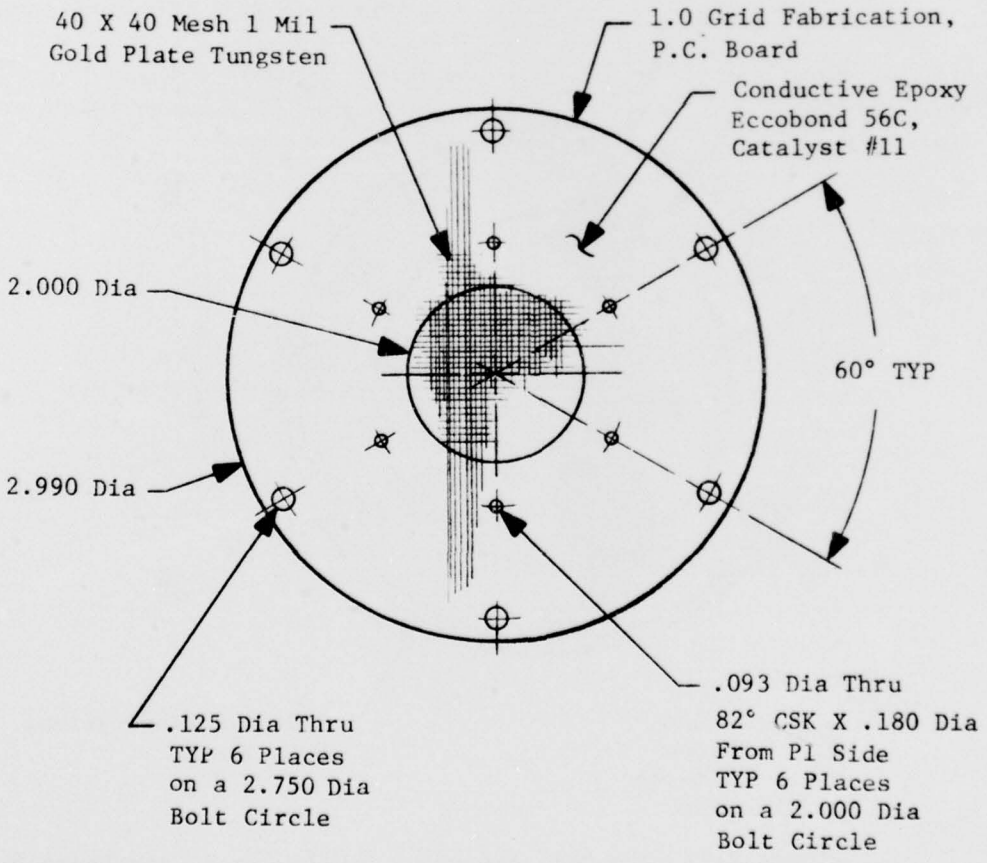


Figure XIV 1.0 Grid Assembly 3.0 Planar Sensor Phase 2